Design and Measurements of a 210 GHz Subharmonically Pumped GaAs MMIC Mixer

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Abstract

A MMIC mixer chip incorporating a separately biased pair of antiparallel GaAs air-bridge Schottky diodes has been developed and tested at 210 GHz. The MMIC wafer is housed in a simple crossed waveguide mount with E-plane coupling probes to couple in the 105 GHz local oscillator and the 210 GHz signal. RF and intermediate frequency matching and filtering is provided on chip as well as separate DC bias paths for each diode. The MMIC chip is described and the measured mixer performance is presented. The measured noise and conversion loss are within 3.5 dB of the best reported subharmonic mixers using individually optimized and mounted planar or whisker contacted diodes at this frequency. The performance of a set of antiparallel diodes, identical to those used in the MMIC but flip chip mounted in a non MMIC subharmonic mixer mount, is also presented and compared with planar diodes made with a different anode deposition process in the same mixer mount.

Introduction

Millimeter-wave monolithic integrated circuits (MMIC's) offer substantial advantages in the production of many high frequency components because of their ability to incorporate both active and passive structures on a single substrate. The development of high quality low parasitic millimeter-wave planar air-bridge Schottky barrier diodes [1,2] has enabled us to push MMIC mixer and varactor multiplier structures well beyond 100 GHz. In this short paper we present early design, fabrication and performance information on a 210 GHz subharmonically pumped GaAs MMIC mixer using two individually biased antiparallel diodes in a simple crossed waveguide mount. The measured mixer performance compares favorably to similar structures which use separate individually optimized and mounted diodes. We conclude with a brief discussion of the measured results and possible avenues of improvement.

MMIC Mixer Chip and Mount Design

The MMIC block diagram is given in Fig. 1 and the top conductor pattern is shown in Fig. 2. Processing is done on quarter wafers of MBE grown GaAs which consist of a 2×10^{17} cm^{-3} n-doped epitaxial layer over a 2.5 μm thick n+ layer doped to 4×10^{18} cm^{-3} on a semi-insulating GaAs substrate mechanically lapped to a thickness of 100 μm. There are a total of 127 steps in the photolithographic process which includes the formation of planar air-bridge Schottky barrier diodes with anodes as small as 1 μm, Si_3N_4 capacitors and plated through via holes. The bottoms of all coplanar ground planes, capacitors, transmission lines and the areas on the backside of the chip, including via holes, are formed with 5000 Å of evaporated Ti/Au followed by at least 2 μm of electroplated gold to lower the resistance and allow soldering and wire bonding on the chip. During processing the active epitaxial layers (n and n+) are removed everywhere except under the diodes (anode and cathode) and a nearby mesa by reactive ion etching. The narrow air bridge to the anode is formed between the anode and a second mesa and larger air bridges are formed from the tops of both mesas to the substrate. The diode air-bridge is formed in the final stage of processing (after all n+ material has been removed) using a photoresist process. Each chip is 1250 μm wide x 2950 μm long and has gold metallization on both the top and bottom surfaces.

The MMIC circuit implements a subharmonic mixer structure [3,4] (local oscillator frequency at one half the signal frequency) with separately biasable antiparallel diodes realized in a planar form with air bridge contacts to the anodes. The mixer circuitry for coupling in and isolating the signal (RF) and local oscillator (LO) and coupling out the down converted intermediate frequency (IF) is realized using coplanar transmission lines (symmetrical ground planes on the top surface of the chip) rather than microstrip to simplify layout and avoid the restriction of having to work with a very thin substrate. A total of 8 bypass capacitors are used for filtering and coupling and 30 via holes connect the top and bottom substrates to block the propagation of modes within the GaAs.

Two RF matching circuit variations were produced; one presents 50 ohms to both the diodes and the other presents a conjugate match to 100 ohms in parallel with 30 fF. Individual RF filtered DC bias lines are provided for each diode by a series of bypass capacitors and open and short circuited stubs. The stubs produce a short at the LO frequency and an open at the RF signal frequency. The IF filter passes DC and IF while presenting an open circuit to the LO. An IF short is provided on the RF side of the diodes by the three bias filter capacitors which have values of 0.2, 12 and 80 pF respectively. The RF/LO diplexer is composed of quarter wavelength sections of alternating high (58Ω) and low (28Ω) impedance transmission lines and provides a pass for the LO and IF and a short for the signal on the LO side of the diodes. A DC return for the diode unbalance current must be provided in the external IF load. LO coupling is provided by an E-plane waveguide probe formed on the MMIC at the LO side of the RF diplexer. The probe is designed to couple into a full height WR-10 rectangular guide with the broad wall of the probe perpendicular to the direction of propagation and extending halfway across the guide. The ground plane on the bottom of the substrate is, of course, discontinued under the probe. The RF signal is coupled in from a similar probe which is formed by a 25 μm thick 150 μm wide gold ribbon separately soldered to the end of the impedance matching line on the RF side of the diodes.

The air-bridge Schottky barrier diodes are formed as an antiparallel pair and have an anode diameter of 2 μm, a center to center separation of 50 μm and an air bridge length of approximately 12 μm. Using test diodes on the MMIC wafer, the average zero bias junction capacitance for the 2μm diameter anodes was measured to be 4.7 fF and the average series resistance (using a four probe measurement at the diode terminals) was found to be 6.5Ω. Due to the thin epitaxial layer the diodes are fully depleted at zero bias and hence have very little reverse bias capacitance variation. Diode ideality factor, barrier height and saturation current averaged 1.35, 0.9 V and 5×10^{-13} Amps respectively.

A waveguide mixer mount was constructed to hold the MMIC chip and to provide the proper LO and RF coupling, DC bias connections and IF removal. The block was fabricated using a crossed guide arrangement with the LO waveguide (WR-10) wire electro-discharge machined through the block perpendicular to the plane of the MMIC chip. The block was then split in half along the plane which cuts the top surface of the MMIC (normal to the LO waveguide) and the signal guide was then machined into both halves with the split along the center of the broad wall of the guide. The MMIC lies in a pocket between the LO and RF waveguides with the E-plane coupling probes protruding into the guides on both sides. The IF is coupled out through a 150 μm wide 50 ohm shielded quartz microstrip line to a K connector at the edge of the block. Biasing is accomplished in a similar way using separate channels machined into the block between the waveguides. The three connections to the MMIC (IF, bias 1 and bias 2) are made by short wire bonds. The chip itself is held in place in the block using 90° C solder. LO is injected via waveguide and RF is injected through a Pickett/Potter dual mode conical feed horn [5]. Backshorts behind both waveguide coupling probes help with LO and RF matching.

MMIC Mixer Performance

The performance of the MMIC mixer over the nominal operating frequency range is plotted in Fig. 3 with all parameters (bias, LO power level and backshort position) optimized at each frequency. Diode parameters for this chip are given in the figure caption. Measurements were performed using a computer controlled noise test system similar to one described in [6]. The measurements yield double sideband (DSB) noise and conversion loss but these have been multiplied by two to give single sideband (SSB) numbers for comparison purposes. The IF frequency was swept from 1 to 2 GHz and the results shown are at 1.4 GHz.

The best performance was obtained at 210 GHz where the single sideband mixer noise temperature was 5040K, the conversion loss was 12.7 dB and the real part of the IF output impedance was 95 ohms. For this performance the LO drive power was 8.5 mW which produced a DC current through each diode of 1.2 mA when the bias voltage was set to 0.1V forward for each device. These results are within 3.5 dB of the best reported subharmonically pumped mixer performance at this frequency [7] and are extremely encouraging considering the complexity of the MMIC chip when compared to more traditional millimeter wave mixer circuits.

Discussion

Several interesting observations were made during the course of this work which deserve mention. First, initial assembly and mounting of the MMIC in the waveguide block proved more difficult than anticipated and several chips were destroyed during this process including all of the RF matched devices. The results shown in Fig. 3 are for a chip which presents a 50 ohm generator impedance at the diode terminals and, as you can see, the performance is rather narrow band. There is some indication, from work on other MMIC structures at Martin Marietta, that the narrow band response may be due, at least in part, to too large a via hole spacing (slightly less than $\lambda_g/2$ for this design).

Second, the air-bridge diodes fabricated by this MMIC process had evaporated titanium-platinum-gold anodes. This is in contrast to the University of Virginia millimeter wave diode process which uses electroplated platinum/gold on GaAs contacts. There is a marked difference in measured ideality factor, barrier height and saturation current between the two types of diodes with the MMIC diodes having consistently higher ideality factors (1.3 rather than 1.1), lower barrier heights (0.9 rather than 1.1V) and greater saturation current (10^{-13} rather than 10^{-17}A). It is not known whether or not these parameters are critical to the mixer performance but as a direct comparison a set of MMIC diodes were diced out of the wafer and mounted in a mixer block designed for University of Virginia planar antiparallel diodes. The mixer performance using the Martin Marietta evaporated anode diodes in the non MMIC mixer mount is also given in Fig. 3. Although the frequency behavior is quite different there is only a small improvement in overall performance using the separately mounted diodes over the full MMIC chip. When University of Virginia diodes with similar cutoff frequencies are used in this block the mixer noise and loss are about 3 dB lower than that obtained with the MMIC diodes. Although one might conclude that there was a significant advantage in the University of Virginia diodes cross comparisons of this type must be made with extreme caution as there are many variables (diode physical size, placement, finger length, parasitic capacitance etc.) which are not held constant in the two cases.

Finally, there seemed to be an optimum combination of LO power, bias current in the diodes and bias voltage at any given LO and RF backshort position which produced the lowest noise and conversion loss. This is not entirely obvious as one would tend to conclude that LO power and bias voltage could be traded off to give the same noise performance so long as the DC current level remained constant in the diodes. This did not occur in practice and as the forward bias voltage was increased on each diode the available gain (into a matched load) began to degrade slightly regardless of the pump power level or induced diode current flow. The effect was not large but it was noticeable.

Summary

The design and performance of the first 200 GHz subharmonically pumped MMIC mixer was presented. The mixer noise and conversion loss were very respectable although somewhat higher than the best non MMIC structures at this frequency. The performance is very narrow band and indicates that further work on the MMIC RF circuitry and possibly reduced via hole spacing are required. There is some indication that the MMIC performance may be improved by changes in the diode physical characteristics as indicated by a comparison of the Martin Marietta evaporated anode diodes with the University of Virginia electroplated anode diodes in a non MMIC mixer block. The availability of independent biasing of the diodes helps in monitoring, in current balancing and in reducing the strong dependence of performance on LO power level. Finally, there appears to be a slight tradeoff between LO power and DC bias for the same diode current flow with these devices.

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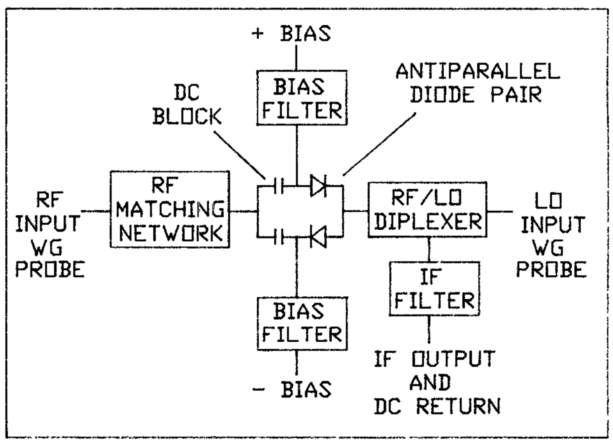

Fig. 1 Block diagram of the 210 GHz MMIC mixer. The bias filters present short and open circuits to the diodes at the LO and RF frequencies, respectively, and pass DC with 3 bypass capacitors to ground. The RF/LO diplexer presents a short circuit to the diodes at the RF frequency and passes the LO and IF frequencies and DC. The IF filter presents an open circuit at the LO frequency and passes IF and DC.

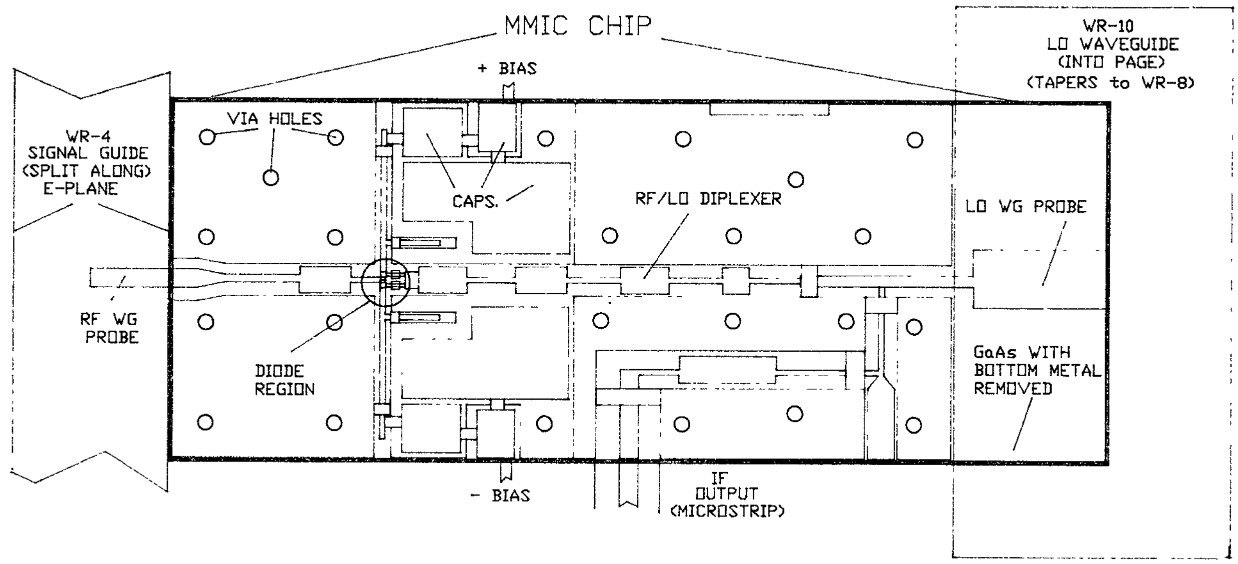

Fig. 2 Top view of the MMIC mixer chip. Chip dimensions are 1250x2950x100μm thick. Backside metallization is discontinuous under the LO probe. A separate 150μm wide gold ribbon is added on the RF input line to couple with a WR-4 waveguide. Bias and IF connections are made through wire bonds to appropriate microstrip channels in the waveguide block.

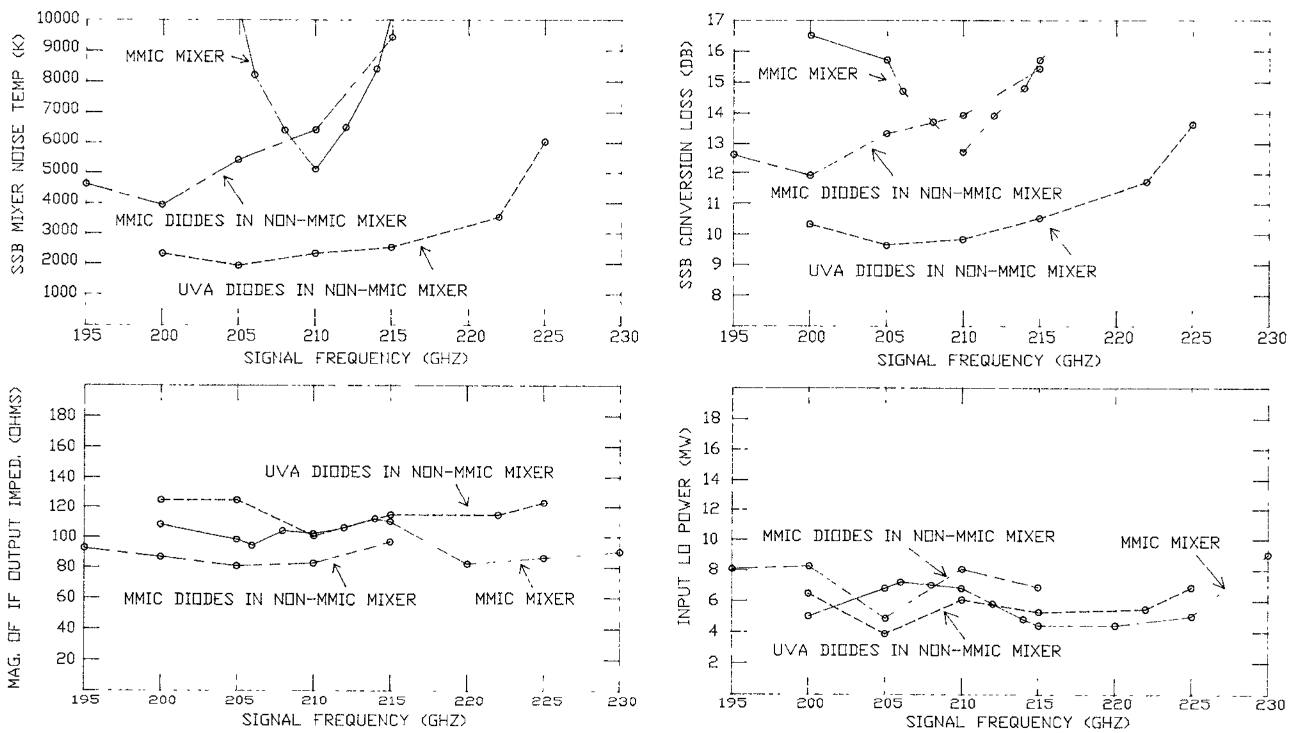

Fig. 3 Measured room temperature mixer noise, conversion loss, magnitude of the IF output impedance and required LO power between 195 and 230 GHz for the MMIC mixer. Results are given for an IF frequency of 1.4 GHz. The mixer was optimized for lowest noise temperature at each frequency using the two backshorts, LO power and separate DC bias in each diode. The noise and conversion loss are measured between the input RF signal feed horn and the IF output K-connector. LO power is referenced to the mixer block input flange. In all cases, SSB values were obtained by doubling the measured DSB results. Also plotted are results for the MMIC diodes mounted in a non-MMIC subharmonic mixer block [7] and results obtained using similar sized Univ. of Virginia planar in the same mixer block. Parameters for all three sets of diodes are as follows:

MMIC chip: **(A)** C_{j0}=4.7 fF η=1.26 R_s=13.6Ω I_s=1x10^{-13}A ϕ_b=.88 **(B)** C_{j0}=4.7 fF η=1.26 R_s=13.6Ω I_s=2x10^{-13}A ϕ_b=.86
MMIC diode: **(A)** C_{j0}=4.7 fF η=1.35 R_s=12.8Ω I_s=3x10^{-13}A ϕ_b=.91 **(B)** C_{j0}=4.7 fF η=1.19 R_s=14.2Ω I_s=3x10^{-14}A ϕ_b=.87
UVa diode: **(A)** C_{j0}=3.0 fF η=1.28 R_s=10.7Ω I_s=3x10^{-16}A ϕ_b=1.1 **(B)** C_{j0}=3.0 fF η=1.25 R_s=12.0Ω I_s=1x10^{-16}A ϕ_b=1.1
Note: C_{j0} is a nominal value and R_s is measured through the IF system and is ~3Ω higher than the value at the diodes.